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Conceptual Design of The Clock System for The MINOS Near Detector

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1. Introduction

The front end electronics for the MINOS Near Detector has two parts. The MINDER Crate is a 6U crate that is located close to the MUX Boxes. This crate contains the QIE Digitizers, which operate with a 53 MHz clock. When data is digitized, it is held in local memories on boards that reside in the crate, called MINDER Modules. After data is acquired, it is transferred from these memories to boards called MASTER Modules, which reside in VME Readout Crates. In each of these crates, there also resides a VME Processor. After data is sent to the MASTER Module, it is processed and stored locally, pending readout by the processor. A description of the system components and the principles of operation are given in [1].

The front end electronics has a Clock System, which provides timing and control for both the VME Crate and the MINDER Crate. This note describes the essential features and operation of the Clock System.

The Clock System has three primary components. They are:

- **The Master Clock**

  This Master Clock is the source of all global timing signals in the system. It receives signals from the Fermilab Accelerator, and processes them to form timing signals needed to operate the electronics. The timing signals are fanned out to the VME Crates and the MINDER Crates. There is one Master Clock in the system, although it has several sub-components.

- **The VME Timing Module (VTM)**

  The VME Timing Module resides in the VME Readout Crate. It receives timing signals from the Master Clock, and processes them to form timing and control signals needed to operate the MASTER Modules. The VTM sends the processed signals out onto the backplane of the VME Crate, and are received by the MASTER Modules and the VME Processor that reside in the crate. There is one VTM in every VME Readout Crate.

  The VTM also contains an interface to the Global Positioning System (GPS) Receiver. The GPS is used to synchronize the timing of events in the Near and Far Detectors. The GPS outputs time words on a periodic basis. The VTM receives the GPS time words, and latches them to record the time of a spill using signals from the Master Clock. The GPS information can then be read out as part of the data acquisition operation, to include absolute time information along with the data from the spill.

- **The MINDER Timing Module (MTM)**

  The MINDER Timing Module resides in the MINDER Crate. It also receives signals from the Master clock. The signals are processed and sent to the MINDER boards in the crate using point-to-point connections. The MTM also has an optional output port, which can be used to send signals to another MINDER Crate that might reside in the same electronics rack. This feature is provided to help reduce the cable plant between the Master Clock and the MINDER Crates. There is one MTM in every MINDER Crate.

A block diagram is shown in Fig. 1. The functionality of these components, and a description of the timing signals, are described in the sections that follow.

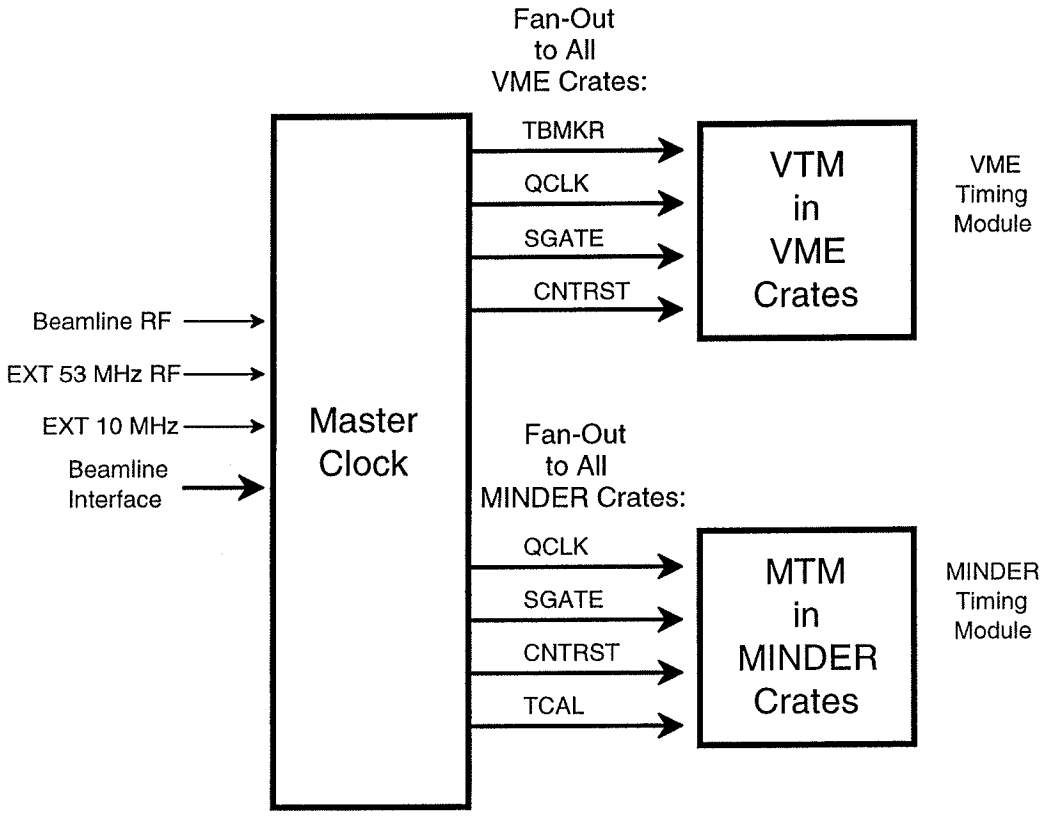

Fig. 1. Block Diagram of Clock System

2. Description of the Primary Timing Signals

The following is a description of the primary timing signals used by the front end electronics:

A. QIE Clock (QCLK)

The Master Clock provides QCLK to both the VME Readout Crate and the MINDER Crate. It operates at a frequency of 53 MHz, which is also the frequency of operation in the Fermilab beam lines. In the MINDER crates, it provides the following functions: it is used for clocking the QIEs, to integrate charge from the photodetectors; it is used for forming timestamps on the data; it is used at half the frequency to transfer data from the MINDER Modules to the MASTER Module. In the VME Readout Crate, the MASTER Modules use the signal at half the frequency to process the data.

The QCLK shall be derived from one of three external input sources: the Fermilab Accelerator; a free-running external 53 MHz clock; or a 10 MHz clock from the GPS Receiver. The choice of which clock to use is an option for the experiment. In addition, it is desirable for the Master Clock to have an on-board 53 MHz clock, which can be used if neither the accelerator clock nor an external clock is available (for example, in test stands.)

In the case where the RF clock from the accelerator is used, it is desirable to have the ability to control the phase of QCLK with respect to the actual accelerator RF. The adjustment shall be implemented on a global basis (one adjustment for the entire system.) The adjustment shall be programmable, and have a range up to one clock cycle, with a step size of 1 nS. In addition, the fan-out of the Master Clock shall have the capability to adjust the phase of the individual outputs. The adjustment range shall be up to one RF clock cycle, in 1 nSec steps.

Because the QIE Clock is used to generate timestamps for an event, QCLK must be a precision signal. The cables must be timed to within 1 nSec over the entire system.

B. Spill Gate (SGATE)

The Master Clock provides SGATE to the front end instrumentation in the MINDER Crates, indicating when a spill occurs. This is used to configure a special state in the front end electronics, for acquiring data from the spill. The Spill Gate is derived from signals received from the Fermilab Accelerator.

The Spill Gate must occur approximately 5-10 uS in advance of the actual spill, so that the front ends can initialize properly. The Spill Gate signal must stay asserted while the spill is in progress, and be de-asserted after the spill is over. It is desirable to have the ability to control the global phase of SGATE (both leading and trailing edges) with respect to QIE Clock. The adjustment shall be programmable, and have a range up to one clock cycle, with a step size of 1 nS. In addition, the fan-out of the Master Clock shall have the capability to adjust the phase of the individual outputs. The adjustment range shall be up to 3 RF clock cycles, in 1 nSec steps. This corresponds to the time-of-flight through the detector, in case such an adjustment is needed.

Because the Spill Gate is used to generate the first timestamp for a spill period, SGATE must be a precision signal. The cables must be timed to within 1 nSec over the entire system.

C. Counter Reset (CNTRST)

The Master Clock provides CNTRST to the front end instrumentation in the MINDER Crates, where it is used to reset the counters that form the timestamps. The counters are zeroed by this signal, and then advanced with subsequent QIE Clocks.

The CNTRST signal must occur at regular intervals in time. It may be implemented using one of two techniques: arranged so that it occurs every N QIE Clocks (phased to QCLK); or arranged so that it occurs periodically in time (using another timing source such as a precision oscillator.) The time interval shall be programmable. The maximum period shall be ~2.5 seconds (1.3E8 QIE Clocks), and the minimum period shall be ~0.1 seconds (~5E6 QIE Clocks.) This gives approximately 5 bits of dynamic range, with a step size resolution of ~0.1 seconds.

It is desirable to prevent CNTRST from occurring during a spill. This could happen unless special precautions are implemented, since the spills do not occur exactly periodically in time. In addition, it is desirable to prevent CNTRST from occurring while data is being transferred and processed after a spill. The interval in which data is being transferred and processed is called the ***Transfer Time***. It is approximately 300 uSec long (for Single-Turn Extraction.) The Master Clock shall generate an internal gate (of programmable duration) after SGATE is de-asserted, which corresponds to the Transfer Time. The period in which the MASTER Module may not generate CNTRST is the interval between the beginning of SGATE and the end of the Transfer Time. This is called the ***Hold-Off Time***. CNTRST is issued promptly if it occurs outside of this interval. The Master Clock must delay the generation of CNTRST if the normal timing of it occurs while the Hold-Off Time is active. In that case, the Master Clock shall

generate CNTRST no sooner than 10 uSec after but no longer than 20 uSec after Hold-Off Time is de-asserted.

The CNTRST signal shall be asserted for one entire clock period (19 nS), and then de-asserted. It is desirable to have the ability to control the global phase of CNTRST with respect to QIE Clock. The adjustment shall be programmable, and have a range up to one clock cycle, with a step size of 1 nS. In addition, the fan-out of the Master Clock shall have the capability to adjust the phase of the individual outputs. The adjustment range shall be up to 3 RF clock cycles, in 1 nSec steps.

Because the Counter Reset signal is used in the generation of timestamps, CNTRST must be a precision signal. The cables must be timed to within 1 nSec over the entire system.

D. Timing Calibration (TCAL)

The Master Clock provides TCAL to the front end instrumentation in the MINDER Crates, where it can be used for a variety of calibration operations. Some of the uses might be: to fire a precision charge injection circuit; to fire the light injection system; to fire the dynode discriminators in a local crate; to fire the dynode discriminators globally over the entire detector.

TCAL can be arranged to occur at regular intervals in time, turned on and off by commands from Run Control. It may be implemented using one of two techniques: arranged so that it occurs every N QIE Clocks (phased to QCLK); or arranged so that it occurs periodically in time (using another timing source such as a precision oscillator.) The time interval shall be programmable. The maximum period shall be ~3 seconds (~1.6E8 QIE Clocks), and the minimum period shall be ~1 mSec (~5.3E4 QIE Clocks.) This gives approximately 12 bits of dynamic range, with a step size resolution of 1 mSec.

Like CNTRST and TBMKR, it is desirable for TCAL not to occur during a spill. This should be prevented using the same techniques as described above.

The TCAL signal shall be asserted for one entire clock period (19 nS), and then de-asserted. It is desirable to have the ability to control the global phase of TCAL with respect to QIE Clock. The adjustment shall be programmable, and have a range up to one clock cycle, with a step size of 1 nS. In addition, the fan-out of the Master Clock shall have the capability to adjust the phase of the individual outputs. The adjustment range shall be up to 3 RF clock cycles, in 1 nSec steps.

Since TCAL is to be used in the calibration of timestamps, then it must be a precision signal. The cables must be timed to within 1 nSec over the entire system.

E. Time Block Marker (TBMKR)

The Master Clock provides TBMKR to the VME Readout Crates, where it is used to form Time Blocks of data. A Time Block is defined as the data set that is collected in a certain period of time, having a common beginning time and a common ending time over the entire detector. There are two buffers on each MASTER Module. While data is being written into one of them, the VME Processor can have access to the data in the other. When the Time Block Marker is received in the VME Readout Crate, the buffers switch state: one goes from reading to writing, and the other goes from writing to reading. This creates blocks of data that are framed in time over the detector, and aids in forming triggers and reconstructing events in the DAQ System.

The TBMKR signal must occur at regular intervals in time. It may be implemented using one of two techniques: arranged so that it occurs every N QIE Clocks (phased to QCLK); or arranged so that it occurs periodically in time (using another timing source such as a precision oscillator.) The time interval shall be programmable. The maximum period shall be 255 mSec (~1.35E7 QIE Clocks), and the minimum period shall be 1 mSec (~5.3E4 QIE Clocks.) This gives approximately 8 bits of dynamic range, with a step size resolution of 1 mSec seconds.

It is desirable to prevent TBMKR from occurring during a spill. As with CNTRST, since the spills are not periodic in time, the generation of TBMKR could occur during a spill unless special precautions are implemented. The MASTER Module must not generate TBMKR during the Hold-Off Time (see the definition of Hold-Off Time in the description of CNTRST above.) TBMKR is issued promptly if it occurs while the Hold-Off Time is not active. The Master Clock must delay the generation of TBMKR if the normal timing of it occurs while the Hold-Off Time is active. In that case, the Master Clock shall generate TBMKR no sooner than 10 uSec after but no more than 20 uSec after the Hold-Off Time is de-asserted. In the rare case where both CNTRST and TBMKR occur during the same clock cycle, the Master Clock may treat them independently; these signals do not interact with each other in the front end system.

The time structure of the TBMKR signal shall have a 50% duty cycle. It shall alternate states with every TBMKR period. This provides easy identification of the state of the readout buffers across the system.

The Time Block Marker does not need to be a precision signal, since it is not used in the formation of timestamps. It is sufficient for the signal to be timed to within 200 nSec over the entire system. It is not necessary to control the phase of TBMKR with respect to QIE Clock.

3. The Master Clock

A. Brief Description

In the current plans for the design of the clock system, the Master Clock design would be based on the systems built for CDF and D0. See [2-4] for descriptions of these systems.

The Master Clock is the source of all of the primary timing signals described in Section 2 above. Some are generated from inputs received from the Fermilab Accelerator. Others may be generated from a precision oscillator or external pulse generator.

The Master Clock is a small system, and resides in a 9U x 400mm VME crate of its own. It has three logical subcomponents, as shown in Fig. 2. The system needs an interface to the beamline clock system. {At this writing, the beamline clock system is not yet designed. It is presumed to be similar to the Tevatron Beam Sync Clock, or TVBS, as described in the references.} The Beamline Interface handles the receiving and decoding of timing information and clocks from the Fermilab Accelerator. The outputs of the Beamline Interface are sent to the Clock System Processor, which generate the primary timing signals needed for the experiment. The primary timing signals are sent to the Clock Fan-Out, where they are distributed to the front end electronics.

The following sections describe the input and output characteristics, as well as the control interface to the experiment.

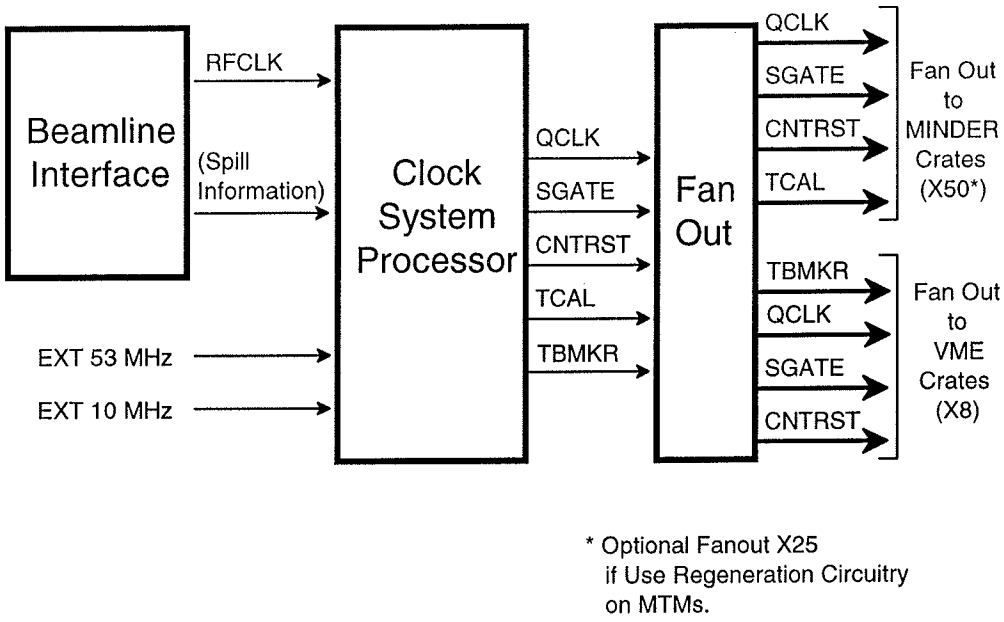

Fig. 2 Block Diagram of Master Clock

B. Input Signals

The Master Clock receives the following signals as inputs to the system:

1. 53 MHz RF from the Accelerator (TEV_RF)

   The 53 MHz RF from the Fermilab Accelerator . It is the fundamental signal used in all of the Fermilab beam lines.

2. Beamline Interface Signals

   The Beamline Interface provides information about the spill. The signals are used to generate an indicator of when the spill is in progress. The Spill Gate must be generated in advance of the actual spill (see Section 2,) so that the front end electronics can initialize properly. The Master Clock may use the Beam Pick-up signals along with control information from the Beamline Interface to achieve this.

3. External 53 MHz CLK (EXT_CLK)

   In the operation of MINOS, it may be desirable to use a non-phased 53 MHz clock for acquiring data. The detector has certain features that tend to randomize the data acquisition, and it may be desirable not to lock the phase of the clock used by the QIEs to the accelerator RF. The choice of which RF source to use is an option for the experiment. In addition, the external clock may be used for test stands, and other applications outside of the accelerator environment. The EXT_RF signal should be provided as a separate input to the front panel of a module, to make it easy to access.

4. 10 MHz RF from the GPS System

   When a non-phased clock is used, a convenient source is the GPS system, which provides a 10 MHz clock as an output. The Master Clock can receive this signal, and has circuitry that boosts the frequency to 53 MHz using phase-lock techniques. The 10 MHz RF signal shall be provided as a separate input to the front panel of a module, to make it easy to access.

5. Internal 53 MHz CLK (INT_CLK)

   As an added feature, it is desirable for the Master Clock to have an internal 53 MHz oscillator, in case neither the accelerator RF nor an external clock source is available.

C. Output Signals

The Master Clock generates the following signals in response to the Input Signals, as described in Section 1:

1. QIE Clock (QCLK)

   The QIE Clock is a 53 MHz, periodic signal with 50% Duty Cycle. It should have ~ 1 nS rise and fall times. It is desirable to have a global phase adjust, in 1 nS steps over 1 clock period. It is also desirable to have the ability to adjust QCLK at the fan-out level, in 1 nS steps over 1 clock period.

   QCLK is fanned out to the instrumentation racks that contain the MINDER Crates. The fan-out shall be point-to-point connections. Each MTM is capable of receiving QCLK directly from the Master Clock. There are approximately 50 crates in the system, with MINDER Crates in each MINDER Rack. As an option to reduce the cable plant, QCLK can be sent to only one MTM in each rack. The MTM can then retransmit the signal to the other MINDER Crate in the rack.

   QCLK is also fanned out to the racks that contain the VME Readout Crates. The fan-out shall be point-to-point connections, one cable to each crate. There are approximately 8 racks in the system, and there is 1 VME Crate in each VME Rack. QCLK is received by the VTM that resides in the crate.

   The logic family for the transmission shall be LVDS. The cable has not been specified, but it is desirable to bundle this signal with the others that fan out from the Master Clock to the MINDER Crates. Mass-terminated cable is preferred, but the quality of the signal transmission and the minimization of skew cannot be compromised.

2. Spill Gate (SGATE)

The Spill Gate is a non-periodic signal, as described in Section 2. It occurs only when there is a spill. It should have ~ 1 nS rise and fall times. It must be asserted 5-10 uSec before the spill, so that the front end electronics can initialize properly. It should be de-asserted within 10 uS after the spill is over, but not before the spill has ended. It is desirable to have a global phase adjust, in 1 nS steps over 1 clock period. It is also desirable to have the ability to adjust SGATE at the fan-out level, in 1 nS steps over 3 clock periods.

It is desirable to have a mode in which the Master Clock can generate a pseudo Spill Gate. This would be useful when the Fermilab Accelerator is not in operation. This could be a periodic pulse, with approximately the same period and duration as the real Spill Gate.

As with QCLK, SGATE is fanned out to the racks that contain the MINDER Crates. The fan-out shall be point-to-point connections, one cable to each crate. There are approximately 50 crates in the system, with 2 MINDER Crates in each MINDER Rack. Like QCLK, an option with SGATE is to receive the signal by the MTM in one crate, and retransmit it to the other crate in the rack. It is desirable to have a few extra outputs from the fan-out, to accommodate other needs.

QCLK is also fanned out to the racks that contain the VME Readout Crates. This is needed by the VTM to record the time of the spill, in conjunction with real-time information from the GPS system. The fan-out shall be point-to-point connections, one cable to each crate. There are approximately 8 racks in the system, and there is 1 VME Crate in each VME Rack. QCLK is received by the VTM that resides in the crate.

The logic family for the transmission shall be LVDS. The cable has not been specified, but it is desirable to bundle this signal with QCLK and others that fan out from the Master Clock to the MINDER Crates. Mass-terminated cable is preferred, but the quality of the signal transmission is important.

3. Counter Reset (CNTRST)

The Counter Reset is a periodic signal, as described in Section 2. It should have ~ 1 nS rise and fall times, and a duration of 1 QIE Clock cycle. The period shall be programmable, from 0.1 Sec to 3 Sec, in 0.1 Sec steps (5 bits.) It must have a programmable hold-off that delays it in the case that it naturally occurs during a spill, as described in Section 2. It is desirable to have a global phase adjust, in 1 nS steps over 1 clock period. It is also desirable to have the ability to adjust CNTRST at the fan-out level, in 1 nS steps over 3 clock periods.

Like SGATE, it is desirable to have a mode in which the Master Clock can generate a pseudo Counter Reset, in the event that the Fermilab Accelerator is not in operation. If CNTRST is implemented by counting QCLKs, then the use of either the external RF or internal RF sources would accomplish this.

As with QCLK and SGATE, CNTRST is fanned out to the racks that contain the MINDER Crates. The fan-out shall be point-to-point connections, one cable to each crate. There are approximately 50 crates in the system, with 2 MINDER Crates in each MINDER Rack. Like the others, an option with CNTRST is to receive it by the MTM in one crate, and retransmit it the other crate in the rack. It is desirable to have a few extra outputs from the fan-out, to accommodate other needs.

The logic family for the transmission shall be LVDS. The cable has not been specified, but it is desirable to bundle this signal with QCLK and SGATE that fan out from the Master Clock to the MINDER Crates. Mass-terminated cable is preferred, but the quality of the signal transmission is important.

4. Timing Calibration (TCAL)

TCAL is a periodic signal, as described in Section 2. It should have ~ 1 nS rise and fall times, and a duration of 1 QIE Clock cycle. The period shall be programmable, from 1 mSec to 4 Sec, in 1 mSec steps (12 bits.) It must have a programmable hold-off that delays it in the case that it naturally occurs during a spill, as described in Section 2. It is desirable to have a global phase adjust, in 1 nS steps over 1 clock period. It is also desirable to have the ability to adjust CNTRST at the fan-out level, in 1 nS steps over 3 clock periods.

Like CNTRST, it is desirable to have a mode in which the Master Clock can generate a pseudo TCAL, in the event that the Fermilab Accelerator is not in operation. The same technique used for CNTRST can be used here.

As with QCLK, SGATE, and CNTRST, TCAL is fanned out to the racks that contain the MINDER Crates. The fan-out shall be point-to-point connections, one cable to each crate. There are approximately 50 crates in the system. There are 2 MINDER Crates in each MINDER Rack. Like the others, TCAL is received by the MTM in one crate, and retransmitted to the other crate in the rack. It is desirable to have a few extra outputs from the fan-out, to accommodate other needs.

The logic family for the transmission shall be LVDS. The cable has not been specified, but it is desirable to bundle this signal with the others that fan out from the Master Clock to the MINDER Crates. As before, mass-terminated cable is preferred, but the quality of the signal transmission is important.

5. Time Block Marker (TBMKR)

The Time Block Marker is a periodic signal, as described in Section 2. It should have ~ 1-10 nS rise and fall times, and a duration of 1 QIE Clock cycle. The period shall be programmable, from 1 mSec to 255 mSec, in 1 mSec steps (8 bits.) It must have a programmable hold-off that delays it in the case that it naturally occurs during a spill, as described in Section 2. Phase adjustment of TBMKR is not required.

As with the other signals, it is desirable to have a mode in which the Master Clock can generate a pseudo TBMKR, in the event that the Fermilab Accelerator is not in operation. The same technique used for CNTRST can be used here.

TBMKR is fanned out to the racks that contain the VMR Readout Crates. The fan-out shall be point-to-point connections, one cable to each rack. There are approximately 8 racks in the system. There is 1 VME Readout Crate in each VME Rack. It is desirable to have a few extra outputs from the fan-out, to accommodate other needs.

The logic family for the transmission shall be LVDS. The cable has not yet been specified.

D. Interface to the Experiment

Certain features of the Master Clock are programmable. It is desirable to have the capability to control these features from other processes, such as Run Control. In addition, it is desirable to have the ability to query the Master Clock to check the condition and status. The preferred environment in the experiment is VME. The Master Clock may reside in its own crate, but the use of VME as the environment is desirable as a way to easily interface to the experiment.

The following are desirable features for access from remote processes or other computers:

1. RF Select

   This feature selects which type of RF source is to be used as the input to the Master Clock: accelerator 53 MHz RF; external 53 MHz RF; internal 53 MHz RF; external 10 MHz RF.

2. Global Phase Adjust of QIE Clock

   This feature adjusts phase of QCLK with respect to the RF source. The adjustment shall be in 1 nS steps over 1 clock period.

3. Phase Adjust of QIE Clock at the Fan-Out Level

   This feature adjusts phase of each individual output of QCLK at the fan-out level. The adjustment shall be in 1 nS steps over 1 clock period.

4. Global Phase Adjust of Spill Gate

   This feature adjusts the global phase of the leading and trailing edges (separately) of SGATE with respect to QCLK, in 1 nS steps over 1 clock period.

5. Phase Adjust of Spill Gate at the Fan-Out Level

   This feature adjusts the phase of each individual output of SGATE at the fan-out level. The adjustment shall be in 1 nS steps over 3 clock periods.

6. Generation of Pseudo Spill Gate

   This feature turns on the internal generation of a periodic signal that mimics the Spill Gate, in case the signals from the accelerator are not available. This should include the ability to set the period, from 0.1 Sec to 3 Sec, in 0.1 Sec steps (5 bits.)

7. Period Adjust of Counter Reset

   The period of CNTRST shall be programmable, from 0.1 Sec to 3 Sec, in 0.1 Sec steps (5 bits.)

8. Global Phase Adjust of Counter Reset

   This feature adjusts the global phase of the leading edge of CNTRST, in 1 nS steps over 1 clock period.

9. Phase Adjust of Counter Reset at the Fan-Out Level

   This feature adjusts the phase of each individual output of CNTRST at the fan-out level. The adjustment shall be in 1 nS steps over 3 clock periods.

10. Generation of Pseudo Counter Reset

    This feature turns on the internal generation of a periodic signal that mimics the Counter Reset signal, in the event that signals from the accelerator are not available. If Counter Reset is implemented by counting QCLKs, then it is not necessary to have a separate feature for this.

11. Period Adjust of Timing Calibration

    The period of TCAL shall be programmable, from 1 mSec to 4 Sec, in 1 mSec steps (12 bits.)

12. Global Phase Adjust of Timing Calibration

    This feature adjusts the global phase of the leading edge of TCAL, in 1 nS steps over 1 clock period.

13. Phase Adjust of Timing Calibration at the Fan-Out Level

    This feature adjusts the phase of each individual output of TCAL at the fan-out level. The adjustment shall be in 1 nS steps over 3 clock periods.

14. Generation of Pseudo TCAL

    This feature turns on the internal generation of a periodic signal that mimics TCAL, in the event that the signals from the accelerator are not available. If TCAL is implemented by counting QCLKs, then it is not necessary to have a separate feature for this.

15. Period Adjust of Time Block Marker

    The period of TBMKR shall be programmable, from 1 mSec to 255 mSec, in 1 mSec steps (8 bits.)

16. Generation of Pseudo TBMKR

    This feature turns on the internal generation of a periodic signal that mimics TBMKR, in the event that the signals from the accelerator are not available. If TBMKR is implemented by counting QCLKs, then it is not necessary to have a separate feature for this.

4. The VME Timing Module

A. Brief Description

The VTM is a 9U x 400mm VME board. It resides in the VME Readout Crate. The primary purpose of the module is to control the formation of Time Blocks of data on the MASTER Module, and to control the readout of the buffers. This is accomplished as follows:

The DAQ system collects fragments of data from the entire detector, grouped into intervals of time called Time Blocks. This is done so that the software trigger can process the data that it receives efficiently. The Time Blocks are formed by controlling the length of time that a particular buffer on each MASTER Module is active for writing.

The control of the readout buffers is implemented by the VTM. The module receives the programmable Time Block Marker signal from the Master Clock, and uses it to generate VME Interrupt Requests. The Interrupt Requests are sent across the backplane of the VME crate. The MASTER Modules in the crate "spy" on the Interrupt Request signals, and use them to change state of the buffers. The VME Processor also receives the Interrupt Requests, and uses them to initiate a new cycle for reading data from the buffers. The VTM shall support the VME Interrupt Protocol.

There are two readout buffers on each MASTER Module, and they may be located at different logical VME addresses. It is desirable for the buffer state to be synchronized across the entire crate, so that the VME Processor knows where in address space to read the data for a given Time Block period. To achieve this, the VTM uses two VME Interrupt signals, one for each buffer. (The selection of which of the VME Interrupt Requests to use has not yet been made.) Each Interrupt Request is asserted in alternating fashion, for example: first Interrupt A, then Interrupt B, then Interrupt A, etc. In this way, a particular readout buffer, along with its VME address space, are associated with a particular Interrupt Request. The convention shall be that the assertion of a particular Interrupt Request causes the associated buffer to be put into the "Read" state, with the other buffer put into the "Write" state. Each MASTER Module handles the control of its own buffers based on this convention.

The Time Block Marker signal from the Master Clock is programmable at the system level. It is a periodic signal, except for a special consideration described below. The nominal period is expected to be approximately 50 mS, with a range of 1 mS to 255 mS, in 1 mS steps (8 bits.) This is used to form Time Blocks of data across the entire system.

The Time Block Marker signal is fanned out to all VME Crates in the system simultaneously, so that readout buffers on MASTER Modules change state at the same time. Due to propagation delays, there may be an uncertainty in exactly when a buffer changes state on a given MASTER Module. The uncertainty is on the order of 200 nS across the entire system. The buffers do not change state in such a way as to cause data from a spill to be split between buffers (see below), so this uncertainty affects only data from cosmic rays. The Trigger and DAQ shall ensure that there is sufficient overlap of data fragments at the edges of Time Blocks, so that the loss of efficiency in triggering due to edge effects is reduced.

A second function of the VTM is to provide the system clock for the MASTER Modules. This is accomplished by receiving QCLK from the Master Clock, and by dividing the frequency by a factor of two to generate SYSCLK. This is then sent onto the backplane of the VME crate. SYSCLK is received by the MASTER Modules, and is used to process incoming data. Since the MINDER Modules transfer data at this frequency, the MASTER may not process the data at a faster rate. The divide-by-two circuitry is easily implemented with Phase-Lock-Loop components.

A third function of the VTM is to record real-time information from the GPS system, and make it available to the VME Processor. To accomplish this, the VTM receives signals from the GPS system, and the Spill Gate. The VTM latches the GPS information in coincidence with the leading edge of the Spill Gate, creating a real-time timestamp for the start of the spill. This information can then be read out as part of the spill data, and provides a means of correlating events from the spill between the Near and Far Detectors. It is desirable for the VTM to provide information that correlates the time of QCLK with the GPS time. To accomplish this, the VTM has a timing circuit that is identical to that used on the front end boards. This circuit is a counter, which is cleared by CNTRST and advances with every QCLK. The value of the counter is latched and is stored in a register at the leading edge of the Spill Gate signal. When the GPS information is read as part of the data from the spill, the time of the spill is recorded and made available to the data acquisition system.

The VTM needs to have a VME interface, so that the VME Processor can read out the spill information

B. Input Signals

The VTM receives the following signals as inputs to the system:

1. Time Block Marker (TBMKR)

   The TBMKR is received from the Master Clock. It is received as LVDS.

2. QIE Clock (QCLK)

   QCLK is received from the Master Clock. It is received as LVDS.

3. Spill Gate (SGATE)

   The Spill Gate signal is received from the Master Clock. It is received as LVDS.

4. Counter Reset (CNTRST)

   The Counter Reset signal is received from the Master Clock. It is received as LVDS.

5. GPS Information

   Timing signals are received from the GPS receiver. {The details and nature of the transmission are left unspecified.}

C. Output Signals

The VTM generates the following signals in response to the Input Signals:

1. VME Interrupt Requests

   The VTM receives the Time Block Marker from the Master Clock. In response, it generates one of two VME Interrupts {to be specified.} The VTM alternates between the two interrupts as it receives the TBMKR signal from the Master Clock. All of the MASTER Modules in the crate have their buffers synchronized in this way.

   In the generation of the Interrupt Request signals, the VTM must obey the VME protocols as described in the VME64 Specifications.

2. System Clock (SYSCLK)

   The VTM receives QCLK from the Master Clock, and divides the frequency by 2 to generate SYSCLK. This is sent onto the VME backplane, using user-defined pins {not yet specified.}

D. Interface to the Experiment

The VTM shall have a normal VME interface, so that it can be read by the VME processor. The following information is provided by the VTM through the VME interface:

1. The GPS Time at the Time of SGATE

   {The details are to be specified.}

2. The Counter Value at the time of SGATE

   {The details are to be specified.}

{At this time, no other requirements are specified. The VTM does not need to have any timing adjustments. Because it resides in a VME Crate, it may be desirable to have other capabilities, such as query of status, perform diagnostics, etc.}

5. The MINDER Timing Module

A. Brief Description

The MTM resides in the MINDER Crate. It has a 6U format, although it is not a VME board. The primary purpose of the module is to receive and retransmit the critical timing signals received from the Master Clock.

The MTM receives the signals from the Master Clock via the front panel. It buffers the signals, and then retransmits them. There are two kinds of output, as shown in Fig. 3. In one path, the signals are buffered and retransmitted out the front panel. This feature allows the signals to be daisy-chained between MINDER Crates. In the second path, the signals are retransmitted out the rear of the module. They are sent to the MINDER Modules in the crate using point-to-point connections. A goal with the clock system is to have QCLK, CNTRST, and TCAL be timed across the entire detector. Because the retransmission has inherent delay, it is compensated by having a delay stage in the path of the signals that are retransmitted to the MINDER Modules, as shown in the figure.

B. Input Signals

The MTM receives the following signals as inputs to the system:

1. QIE Clock (QCLK)

   The QIE Clock is received from the Master Clock. In order to reduce the cable plant, it is desirable that it be received on a mass-terminated cable, along with SGATE, CNTRST, and TCAL. The signal is received as LVDS.

2. Spill Gate (SGATE)

   The Spill Gate signal is received from the Master Clock. In order to reduce the cable plant, it is desirable that it be received on a mass-terminated cable, along with QCLK, CNTRST, and TCAL. The signal is received as LVDS.

3. Counter Reset (CNTRST)

   The Counter Reset signal is received from the Master Clock. In order to reduce the cable plant, it is desirable that it be received on a mass-terminated cable, along with QCLK, SGATE, and TCAL. The signal is received as LVDS.

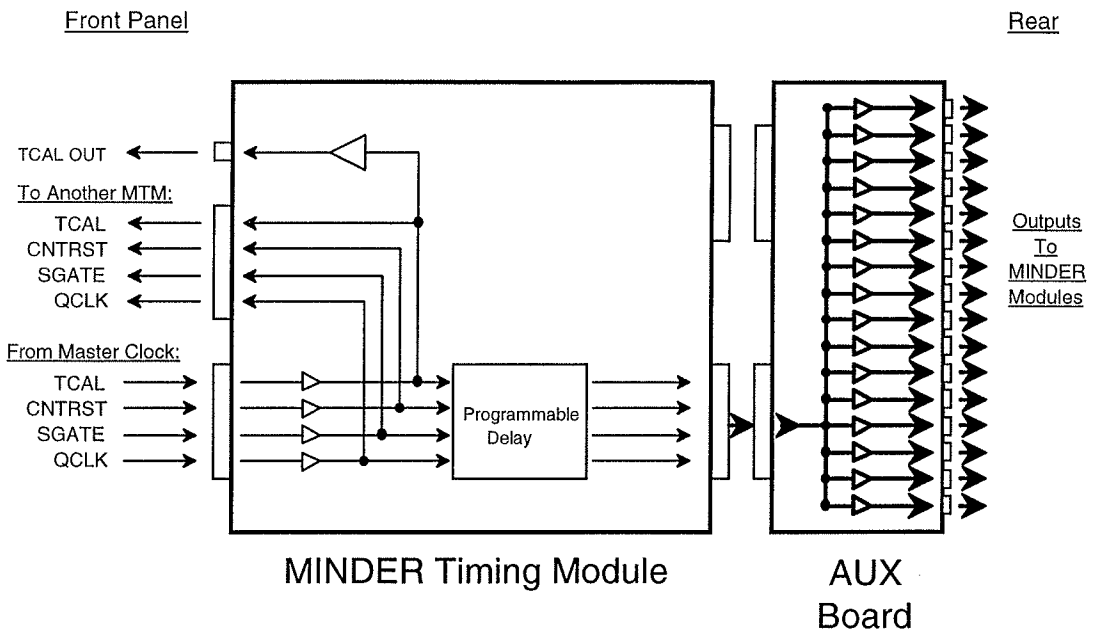

Fig. 3. Block Diagram of the MINDER Timing Module

4. Timing Calibration (TCAL)

   The TCAL signal is received from the Master Clock. In order to reduce the cable plant, it is desirable that it be received on a mass-terminated cable, along with QCLK, SGATE, and CNTRST. The signal is received as LVDS.

C. Output Signals

The MTM receives and buffers QCLK, SGATE, and CNTRST for use by the MINDER Modules. The signals are first delayed by a programmable amount, and then sent out the rear of the module. The signals received by the Transition Modules that service each MINDER Module using point-to-point connections. There are 16 MINDER Modules per MINDER Crate. {At the present time, TCAL is not used by the MINDER Modules.}

The MTM also regenerates QCLK, SGATE, CNTRST, and TCAL, sends them out the front of the module. The signals can be sent to another MINDER Crate. The delay in this path is compensated for using the programmable delays of the signals sent to the MINDER Modules. In the case where two crates are daisy-chained together, the delays in the second crate (the termination end) would be set to the minimum. The delays in the first crate would be adjusted so that the signals are received by the MINDER Modules in the first crate at the same time (to within 1-2 nS) as the signals in the second crate. The delays do not need to be programmable in the sense that they can be controlled through software; they are sent once and then should not need to readjusted.

The MTM shall provide a separate output connector on the front panel for TCAL. This allows the signal to be used locally to fire test pulsers, or to be used by the Trigger Module to test its functionality.

D. Interface to the Experiment

{At this time, there is no interface specified. The MTM does not need to have any timing adjustments. It may be desirable to have the ability to communicate with it through the system, to query the status, perform diagnostics, etc.}

7. Bibliography

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